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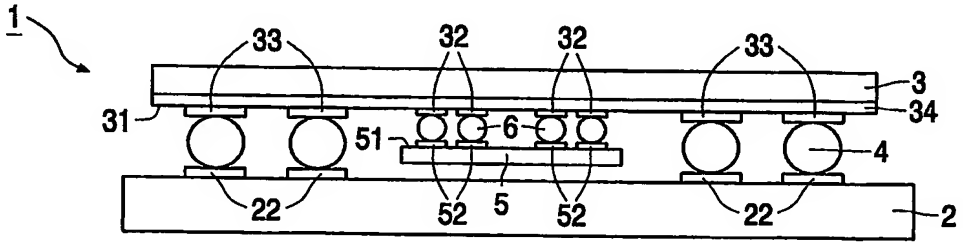
(54) Title: ELECTRONIC DEVICE AND METHOD OF MANUFACTURING A SUBSTRATE



(57) Abstract: Provided is an electronic device (1) with a semiconductor element (5) and a substrate (3) of a material chosen from the group of AlSi, AlSiC, AlSiGe and the like. These materials are provided by providing preferably crystalline particles of a semiconductor material in a thermally conducting matrix material, after which the material is adequately strengthened by a heat treatment. The semiconductor element (5) is a digital integrated circuit with a large number of first contact pad (32) by preference. In such applications, thermal mismatch can easily lead to breakdown of the packaged device. This is prevented through the use of the substrate (3) of the invention.

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Electronic device and method of manufacturing a substrate

The invention relates to an electronic device comprising a semiconductor element and a substrate, each having a first side with first contact pads, which first contact pads are one by one mutually connected, which substrate is further provided with second contact pads for external contacting and interconnect lines, each of which interconnect lines connects a first contact pads with a second contact pad.

The invention also relates to a method of manufacturing a substrate provided with contact pads at a first side thereof.

Such a device is known from US-B-6,300,161. The substrate herein is an interposer substrate that has the function to convert the pitch of relatively narrow spaced first contact pads for contacting those of the semiconductor element, in cause an integrated circuit, to wider spaced second contact pads for external contacting. These second contact pads are connected with solder bumps to conducting pads on a surface of a carrier.

In use thermal cycling will occur due to heat generated during operation of the semiconductor element. To limit stresses due to the thermal cycling it is suggested in the above mentioned patent to use compliant materials, such as silicon and gallium arsenide with similar coefficient of thermal expansion (CTE) to the semiconductor element for the substrate and the carrier.

It is a disadvantage of the proposed materials that their thermal conductivity is limited. An alternative material could of course be used, but there is a further condition that the difference in the coefficients of thermal expansion may not be too large.

It is therefor an object of the invention to provide an electronic device with an improved thermal expansion compensation.

This object is achieved in that the substrate comprises a material obtainable by sintering a matrix of a thermally conducting material, preferably a lightweight metal, in which matrix particles of a semiconductor material are embedded. Particles of a semiconductor material are particularly suitable to be embedded in the matrix material, as they can be wetted well by the metal matrix, probably due to a similar structure of the materials . A suitable adhesion between the matrix material and the generally crystalline

particles is therewith realized. Therefore, stresses that result from unequal thermal expansion of both materials, do not lead to phase separation or microcracks.

Surprisingly, it has been found that the resulting material has a coefficient of thermal expansion that is in the vicinity to that of the semiconductor element, whereas the thermal conductivity is near to that of the matrix material. The coefficient does not need to be more or less the same as that of the semiconductor element, as was suggested in the prior art. Preferably, the substrate has a coefficient of thermal expansion that is larger than that of the semiconductor element, but smaller than that of a carrier, to which the electronic device can be attached.

This insight is derived thereof, that thermal and mechanical mismatch between the substrate and an external body is a risk for failure, which is at least as high as any mismatch between the substrate and the semiconductor element. The reduction of the risk relating to this latter mismatch is due to various developments. First of all, the size of the semiconductor element has been reduced substantially in the previous years. Furthermore, means to overcome mismatch problems such as any underfill for bumps or specific adhesives, are available.

On the other hand, the mismatch between the substrate and an external body has become more important, both due to miniaturization and to enhanced requirements requesting stability at higher temperatures. The external body is herein a carrier, such as a printed circuit board, but may be a cover plate as well. The miniaturization is herein both in lateral directions (small bumps used for interconnection with any carrier), as in vertical directions (thinner devices). The thinness in particularly enhances the need for specific heat dissipation and may reduce inherent mechanical stability. The higher temperatures are a consequence of the use of lead-free solder during processing, but of enhanced use conditions (e.g. in small portable apparatus, that need to function anywhere and wherein cooling means such as ventilators are not desired.

Thus, the devices must be able to withstand higher temperatures, during processing and/or during use. This may not lead to fracture or mismatch with the external body. Besides, there is a tendency to reduce the thickness of the complete device. This enhances the need to counteract thermal mismatches between the substrate and the external body. For these reasons, the invention provides a substrate with a good thermal conductivity and with a thermal coefficient of expansion larger than that of the semiconductor element, and similar to that of the external body.

Suitably, the resulting substrate has a coefficient of thermal expansion in the range from 5.10^{-6} to 15. 10^{-6} /K, particularly in the range from 7.10^{-6} to 13.10^{-6} /K. Experimental results have shown that this results in an excellent thermal expansion compensation. Such a thermal expansion nicely fits between that of the semiconductor element, particularly those based on a Si, Si:Ge, SiC, GaAs, etc. body, and that of a carrier such as a printed circuit board (17.10^{-6} /K), made of glassepoxy. The coefficient of thermal expansion can be tuned through the ratio between the amount of thermally conducting material and the amount of semiconductor material. Preferably the particles of semiconductor material constitute 40-60% by weight of the total.

Particularly preferred materials are Al-Si, Al-SiC and Al-SiGe. Such materials have a low specific weight, a low warpage, a small surface roughness (Ra approximately 1 μm) and high thermal conductivity (K>100 W/mK). While the high thermal conductivity allows the use as the interposer for absorption and withdrawal of heat generated during operation of the semiconductor element, the small surface roughness allows to provide further layers with thin-film processes. Instead of pure Al, an alloy of Al, for instance $Al_{.99}$-$Si_{.01}$ can be used.

In order to provide the contact pads and interconnects on the substrate use can be made of thin-film processing, or eventually of thick film processing, or of lamination of the substrate with a second substrate that includes the desired patterns.

In a further embodiment an electrically insulating adhesive layer is present at the first side of the substrate. This implies that the contact pads are not provided with thin film processing, but attached to the substrate after being defined on another substrate. The adhesive layer is thermally insulating to a certain extent as well. This is not problematic in that the substrate can transport the heat quickly due to the high thermal conductivity. However, if desired, additional measures can be taken to counteract the thermal barrier of the adhesive layer; the adhesive layer is preferably chosen to be thin, which is possible due to the small surface roughness of the substrate. It has for instance a thickness between 10 and 20 μm. Further on, any space between the semiconductor component and the substrate can be filled with a thermal underfill material. This takes away any barrier against thermal transport. Also, at any area that does not contain contact pads, the adhesive layer may be removed, and then be replaced by the thermal underfill. Further on, the adhesive layer can be chosen to have a thermal conductivity that is not too low. Suitable examples are modified acrylic adhesives, such as those commercially obtainable as Du Pont Pyralux. However, any electrically insulating layer with a adhesion strength that is sufficient to prevent peeling off of

the bond pads during bumping and handling, and with a thermal stability as required for the device, can be used as adhesive layer.

It is particularly preferred that the first contact pads are mechanically anchored in the adhesive layer. Such mechanically anchoring is obtainable with the method of manufacturing an interposer substrate, as is discussed below. In such a construction, the contact pads have edges, which are nearly completely surrounded by the adhesive. This has the advantage of increased adhesion strength. The adhesion strength will be further improved by filling the space between the semiconductor element and the interposer substrate. Due to such a filling, the adhesive will be connected also to the filling material. Suitable materials hereto are thermal underfills and underfilling molding material. A preferred example hereof is for instance an acrylate that can be provided as a solid layer, which melts during heating. Such an acrylate has the additional advantage that any bumps used to connect the first contact pads of the semiconductor element and the interposer substrate will not loose their shape during bumping.

As will be clear from the foregoing, the invention is particularly suitable for applications in which a considerable amount of heat must be dissipated, while there are at the outside of the substrate connections with external or internal elements, of which the alignment is critical.

In a first application, the semiconductor element is an integrated circuit and electrical connections between the substrate and both the semiconductor element and an external carrier is provided with bumps. Present day integrated circuits have a high number of first contact pads, generally embodied as a ball grid array. This is particularly the case for integrated circuit for digital consumer applications, and particularly of microprocessors. In many cases the operating frequency of such integrated circuit is particularly high, in the gigahertz range. This leads to a considerable production of heat during operation. With the present invention a low cost ball grid array with an I/O above 1000 and a component size of 40 * 40 mm or less can be realized. The - interposer - substrate in an IC package must not only function as a pitch converter, but also as a CTE converter. In case, due to power cycling, the integrated circuit heats up. The resulting stresses in the interconnect between the integrated circuit and the substrate as well as the interconnect between the substrate and the carrier will stay within acceptable limits in the present invention.

The device of the invention furthermore allows the use of leadfree solder materials, such as $Au_{80}Sn_{20}$ for the bumps for the connection between the substrate and the carrier. In order to be able to use a lead-free solder, the temperature used for the soldering

considerably higher than with convential lead-containing solder. But it has the advantage that in the reflow of the component onto the printed circuit board, the bumps on the IC will not remelt. The device of the invention further allows the use of bumps with a very fine pitch between the semiconductor element and the substrate.

It is particularly preferred that a first capacitor electrode a layer of dielectric material and a second capacitor electrode are provided on top of the substrate. The first capacitor electrode hereof can be realized in the same layer as the first and second contact pads. The resulting capacitors can be used as decoupling capacitors. The advantage of this, in combination with the substrate of the present invention, is that also a dielectric material with a high dielectric constant can be provided. These materials, if application from solution, need a heat treatment after application to the substrate. Besides, as any capacitor, they need a flat surface so that the electric field within the capacitor is not disturbed. According to the invention, there is a substrate that is able to withstand sufficiently high temperatures; besides, the surface of the substrate is relatively flat.

Herein, the substrate is provided with a layer of insulating material. Then an electrode layer and the layer of dielectric material are provided. Patterning occurs in conventional manner, with dry or wet-etching. Subsequently the second conductive layer, the top electrode of the capacitor, can be deposited. Dielectric materials with a high dielectric constant are applied in a sol-gel process by spin-coating of a precursor solution and subsequent conversion in a heat treatment, such as for instance known from EP-A 676384. Suitable materials are among others lead-zirconium-titanates, lead-lanthan-zirconium-titanates, barium-zirconium-titanates.

In a second application the semiconductor element is surrounded by side walls onto which a transparant cover plate is present, and the semiconductor element is an opto-electronic element. Examples of the opto-electronic elements are light-emitting diodes, photodiodes, lasers, image sensors and displays. In this case the substrate has a large surface area, in the order of some cm^2. Even small mismatches in expansion may lead to problems with the cover plate, that is for instance of glass.(remark: no, one can have AlSi 7 and also glass with 7 ppm) Further on, the substrate surface is relatively flat. As a result, any uncontrolled tilt of the component to the substrate is prevented. The good thermal conductivity of the substrate is a further advantage. The miniaturization in these applications takes place in the vertical direction, e.g. all has to be thinner than before. A direct consequence hereof is that the heat must be dissipated more efficiently.

The interconnect lines and the second contact pads at the substrate are preferably present at the first side. The second contact pads may be fitted for bumping, but also for the provision of a flexfoil. This has the advantage that the assembly of the semiconductor elements to the interposer substrate can be done before separating the interposer substrate into individual devices. However, the interconnect lines may extend along side faces, or via through-holes in the interposer substrate. Alternatively, the interposer substrate may have been preformed into a desired shape, and the interconnect lines extend along the first side and a second side of the substrate. In this case the preformed may be realized before or after assembly of the semiconductor element. The material and the dimensions of the interconnect lines are chosen such as to provide desired line impedances. By preference, the interconnect lines comprise Cu and have in cross-section a height of a few micrometers and a width of about 20 microns, resulting in a line impedance of 50 Ohms.

In a further embodiment cooling elements are present at a second side of the interposer substrate that is remote from the first side. These cooling elements may be realized by structuring the interposer substrate at the second side. Alternatively, another material having a similar coefficient of thermal expansion may be provided at this side in a desired structure. Suitable materials are Al-SiC, Ti and NiFe. In another alternative an active cooling element is attached to the second side of the interposer substrate. The active cooling element is for example a heat pipe, preferably made of a material meshing the coefficient of thermal expansion of the interposer.

It is a second object of the invention to provide a method of manufacturing an interposer substrate provided with contact pads at a first side thereof, which has a desired thermal expansion coefficient and can be realized on wafer-scale level. This is achieved in a method comprising the steps of

providing the substrate that comprises a material obtainable by sintering a matrix of a thermally conducting material in which matrix particles of a semiconductor material are embedded;

providing a second substrate comprising a first layer of conductive material, a second layer of a sacrificial layer and a sublayer between said first and said second layer, in which sublayers patterns in conformity with those in the first layer are defined, but with a smaller width;

providing an adhesive layer on either the substrate or the first layer of the second substrate;

assembling the substrate and the second substrate, such that during assembly the first layer faces the substrate; and

removing the sacrificial layer of the second substrate.

With the method of the invention, the assembly of the interposer and its contact pads and other electrically conductive tracks can be done after that the patterns in the conductive tracks have been defined elsewhere. Further on, the method of the invention allows assembly without the need to do any photolithography. From an industrial point of view, this is preferred.

If desired any further layers can be applied with thin-film processing on top of the first layer after removal of the sacrificial layer. Such additional layers may have been provided in the second substrate before assembly. Also, any further layers may be provided on the surface of the interposer substrate before the assembly.

Particularly preferred is a second substrate wherein the first layer comprises copper and the sacrificial layer comprises Al or an aluminum alloy. The sublayer herein is preferable comprised in the sacrificial layer, and made by doing an underetch treatment in an etchant that is selective towards copper. The first layer can have a thickness between about 1 and 30 microns, preferably between 5 and 10 microns. Good results have been obtained with this method, which will be further explained with reference to the figures.

These and other aspects of the device and the method of the invention will be further explained with reference to the figures, in which

Fig. 1 shows schematically and in cross section a first embodiment of the device;

Fig. 2 is a perspective view of the substrate in the device;

Fig. 3 is a diagrammatically cross-sectional view of a second embodiment of the device.

The figures are not drawn to scale and purely schematically. Like reference numbers in different figures refer to like parts.

Fig. 1 shows a device 1 according to the invention which comprises a substrate 3 and a semiconductor element 5, in this case an integrated circuit. The substrate 3 is present on a carrier 2, which is in this case a printed circuit board. The integrated circuit 5 and the substrate 3 each have a first side 51, 31, that are facing each other in this example. First contact pads 52, 32 are present on the integrated circuit 5 and the substrate 3 which are mutually connected by microbumps 6, in this example of $Au_{80}Sn_{20}$. Although the first contact pads 52 are shown to be on top of the surface of the integrated circuit 5, this may be different in practice. The first contact pads 52 could be present beneath apertures in a passivation layer. Alternatively, they can be present on top of the passivation layer, by means of bond pads on active structure, such as known per se.

Interconnect lines (not shown) and second contact pads 33 are present at the first side 31 of the substrate 3 as well. The second contact pads 33 have a mutual width that is larger than the first contact pads 32, and are therefore suitable for external connection to the contact pads 22 on the carrier 2. This is realized in this case with solder balls 4, in case of an $Sn_{.96}$-$Ag_{.03}$-$Cu_{.01}$ alloy. The printed circuit board 2 is for example an epoxy based substrate, with a coefficient of thermal expansion of for example $17x10^{-6}$/K. The integrated circuit 5 has a relatively low CTE of for example $3x10^{-6}$/K. The substrate 3 is preferably made of AlSi or AlSiC with copper (Cu) conductive tracks thereon. AlSi and AlSiC have a CTE in the range between $7x10^{-6}$/K and $13x10^{-6}$/K. It is provided at its first side 31 with a layer of a dielectric 34. Whereas the substrate 3 has for instance a thickness of about 1 mm, the thickness of the layer of dielectric 34 is about 10 μm and has an effective dielectric constant of 4,6. It was provided by spinning a layer or foil lamination. The first and second contact pads 32, 33 are part of a Cu conductor with a width of 15 μm and a thickness of 5 μm is applied. With such choice of the dielectric and the conductor, a control impedance line of 50 Ω can be realized.

Fig. 2 shows a diagrammatically cross-sectional view of a second embodiment of the device 1 according to the invention. In this embodiment, the substrate 3 is provided with a passive cooling element 9 on a side remote from the integrated circuit 5. The cooling element 9 provided with ribs is made out of a material of similar CTA as for example AlSiC, Ti or NiFe. The cooling element 9 is shown to be a separate layer. However, it may be realized in that the substrate 3 is at the side remote of the integrated circuit 5 structured to

obtain an effective cooling. Instead of the passive cooling element, an active cooling element can be attached to this side. The active cooling element is for example a heat pipe made of a material meshing the coefficient of thermal expansion of the substrate 3. Preferable materials are for example Ti and NiFe.

In the embodiment of Fig. 2, the dielectric layer 34 is an adhesive layer in which the first and second contact pads 32, 33 and any interconnect lines present are mechanically anchored. This structure has been realized by the provision of a foil with a first layer and a second layer. The first layer comprises Cu in this case, and the second layer comprises Al. However, other materials can be used as well, if the second layer can be etched selectively with respect to the first layer. Also a third layer in between of the first and the second layer may be present. After patterning the first layer according to the desired pattern including the first and second contact pads 32,33.

Fig. 3 shows a diagrammatically cross-sectional view of a third embodiment of the device 1 according to the invention. The device 1 of this embodiment comprises an opto-electronic element as the semiconductor element 5. In particular, the semiconductor element is a charge-coupled device (CCD). The element 5 is present on a substrate 3 of AlSi. The substrate 3 is provided with a layer 34 of dielectric, which is in this case a glue on acrylate-basis, that is commercially available as Pyralux. On top of the layer of dielectric 34 a conductive layer is present, comprising first and second contact pads 32, 33 and (not shown) interconnectlines. The first contact pads 32, 52 at the first sides 31, 51 of the substrate 3 and the element 5 are connected through wire-bonds 6. To the second contact pads 32 a flex foil 45 is connected. The opto-electronic element 5 is provided in a cavity with side walls 41 and a cover plate 42. The side walls 41 are in this example made of a molded part. This molded part is in this example mechanically fixed and aligned to the substrate 3 through holes 35. The molded part 41 is provided with a metal coating 44 of Al at the outside, in order to increase the moisture resistance. However, this metal coating 44 is not necessary. The cover plate of glass is attached to the side walls 41 with an adhesive 43. Preferably, O-rings are provided in the side walls 41, preferably at the interface with the substrate 3 and at the interface with the cover plate 42 in order to create a hermetically sealing.

In short, provided is an electronic device with a semiconductor element and a substrate of a material chosen from the group of AlSi, AlSiC, AlSiGe and the like. These materials are provided by providing preferably crystalline particles of a semiconductor material in a thermally conducting matrix material, after which the material is adequately strengthened by a heat treatment. The semiconductor element is a digital integrated circuit

with a large number of first contact pads by preference. In such applications, thermal mismatch can easily lead to breakdown of the packaged device. This is prevented through the use of the substrate of the invention.

CLAIMS:

1. An electronic device comprising a semiconductor element and a substrate, each having a first side with first contact pads, which first contact pads are one by one mutually connected, which substrate is further provided with second contact pads for external contacting and interconnect lines, each of which interconnect lines connects a first contact pads with a second contact pad,

characterized in that the substrate comprises a material obtainable by sintering a matrix of a thermally conducting material in which matrix particles of a semiconductor material are embedded.

2. An electronic device as claimed in Claim 1, characterized in that the thermally conducting material is chosen from the group of aluminum and aluminum alloys

3. An electronic device as claimed in Claim 1 or 2, characterized in that the semiconductor material is chosen from the group of Si, SiC, SiGe and Ge.

4. An electronic device as claimed in Claim 1, characterized in that the resulting interposer has a coefficient of thermal expansion in the range from 5.10^{-6} to $15.\ 10^{-6}$ /K.

5. An electronic device as claimed in any of the previous Claims, characterized in that an electrically insulating adhesive layer is present at the first side of the substrate, and that the first contact pads are mechanically anchored in the adhesive layer.

6. An electronic device as claimed in Claim 1, characterized in that:

the semiconductor element is an integrated circuit;

the first contact pads of the substrate and the integrated circuit element are facing each other and mutually connected with bumps; and

the second contact pads and the interconnect lines are present at the first side of the substrate, which second contact pads are suitable for contacting to a carrier that is oriented substantially parallel to the substrate.

7. An electronic device as claimed in Claim 1, characterized in that:

the semiconductor element is surrounded by side walls onto which a transparant cover plate is present, and

the semiconductor element is an opto-electronic element.

8. An electronic device as claimed in Claim 1, characterized in that cooling elements are present at a second side of the interposer substrate that is remote from the first side

9. A method of manufacturing a substrate provided with contact pads at a first side thereof, comprising the steps of

providing the substrate that comprises a material obtainable by sintering a matrix of a thermally conducting material in which matrix particles of a semiconductor material are embedded;

providing a second substrate comprising a first layer of conductive material, a second layer of a sacrificial layer and a sublayer between said first and said second layer, in which sublayers patterns in conformity with those in the first layer are defined, but with a smaller width;

providing an adhesive layer on either the substrate or the first layer of the second substrate;

assembling the substrate and the second substrate, such that during assembly the first layer faces the substrate; and

removing the sacrificial layer of the second substrate.

10. A method as claimed in Claim 9, wherein the substrate is provided in a preformed shape.

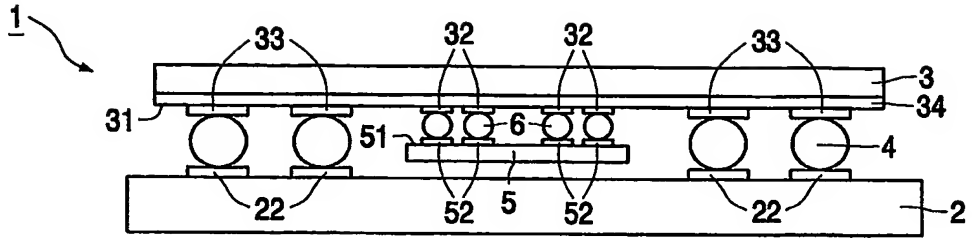

FIG. 1

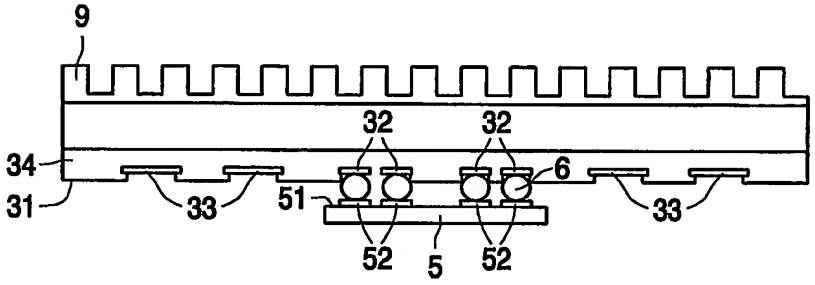

FIG. 2

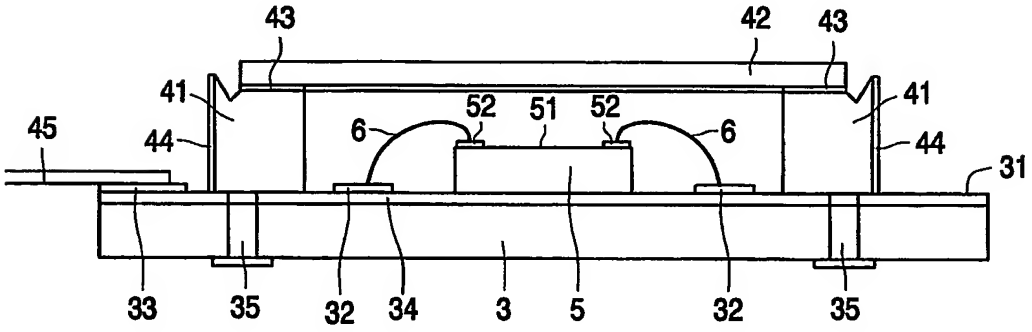

FIG. 3

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

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Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

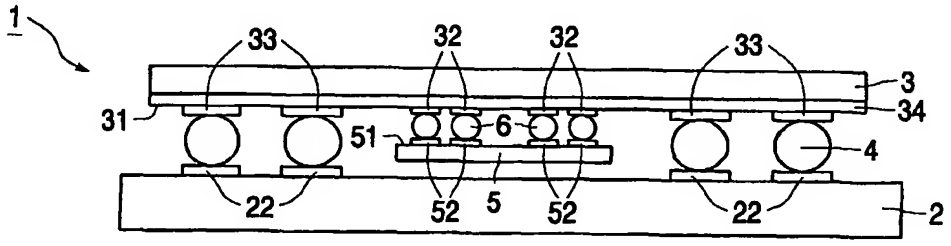
Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: ELECTRONIC DEVICE AND METHOD OF MANUFACTURING A SUBSTRATE



(57) Abstract: Provided is an electronic device (1) with a semiconductor element (5) and a substrate (3) of a material chosen from the group of AlSi, AlSiC, AlSiGe and the like. These materials are provided by providing preferably crystalline particles of a semiconductor material in a thermally conducting matrix material, after which the material is adequately strengthened by a heat treatment. The semiconductor element (5) is a digital integrated circuit with a large number of first contact pad (32) by preference. In such applications, thermal mismatch can easily lead to breakdown of the packaged device. This is prevented through the use of the substrate (3) of the invention.

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(88) Date of publication of the international search report:
20 January 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 03/06345

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/14 H01L23/373

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 262 477 B1 (HOFFMAN PAUL R ET AL) 17 July 2001 (2001-07-17) the whole document	1-3,5-8 4
Y	EP 0 938 137 A (SUMITOMO ELECTRIC INDUSTRIES) 25 August 1999 (1999-08-25) the whole document	4
X	US 5 774 336 A (LARSON RALPH I) 30 June 1998 (1998-06-30) the whole document	1-3
A	US 6 300 161 B1 (GOETZ MARTIN P ET AL) 9 October 2001 (2001-10-09) the whole document	1-8
A	US 5 886 407 A (POLESE FRANK J ET AL) 23 March 1999 (1999-03-23) the whole document	1-8

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 September 2004	22/11/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Le Gallo, T

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 03/06345

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-8

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8

an electronic device comprising a substrate comprising a material obtainable by sintering a matrix of a thermally conducting material in which matrix particles of a semiconductor material are embedded.

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2. claims: 9,10

method for providing contact pads on a substrate comprising a material obtainable by sintering a matrix of a thermally conducting material in which matrix particles of a semiconductor material are embedded.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 03/06345

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